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Newport
South Wales
NP10 8QQ

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Signed P Mahoney

Dated 20 December 2004

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THE PATENT OFFICE
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- 5 MAR 2004
The Patent Office
LONDON

Request for grant of a patent

The Patent Office
Cardiff Road
Newport
South Wales NP10 8QQ

1. Your reference
5484202/JAC

2. Patent Application Number
05 MAR 2004 **0405026.6**

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

Innovision Research & Technology PLC
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Patents ADP number *(if known)* ~~08144784001~~

If the applicant is a corporate body, give the country/state of its incorporation — Country: England
State:

4. Title of the invention
DUAL MODE READER / TAG ARCHITECTURE

5. Name of agent
"Address for Service" in the United Kingdom to which all correspondence should be sent

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Patents ADP number
~~00001826001~~

6. Priority: Complete this section if you are declaring priority from one or more earlier patent applications filed in the last 12 months.

Country	Priority application number	Date of filing

Patents Form 1/77

7. Divisionals, etc: Complete this section only if this application is a divisional application or resulted from an entitlement dispute.

Number of earlier application | Date of filing

8. Is a Patents Form 7/77 (Statement of inventorship and of right to grant of a patent) required in support of this request?

YES

9. Enter the number of sheets for any of the following items you are filing with this form.

Continuation sheets of this form	
Description	3
Claim(s)	1
Abstract	0
Drawing(s)	2+2

10. If you are also filing any of the following, state how many against each item.

Priority documents	NO
Translations of priority documents	NO
Statement of inventorship and right to grant of a patent *(Patents form 7/77)*	1 + 1 COPY
Request for preliminary examination and search *(Patents Form 9/77)*	NO
Request for Substantive Examination *(Patents Form 10/77)*	NO
Any other documents *(please specify)*	NO

11. I/We request the grant of a patent on the basis of this application

Signature _____ Date 5 March 2004

BERESFORD & Co

12. Name and daytime telephone number of person to contact in the United Kingdom

Jane Clark

Tel: 020 7831 2290

Dual Mode Reader / Tag Architecture

1 Background

The growth and diversity of RFID applications and the use of near field communication ("NFC") systems is progressing at an exponential rate. The existing RFID system concepts, based on isolated Reader and Tag functionality, do not necessarily provide the optimum system level solution for an ever-increasing diversity of application areas. Many of these emerging application areas may require each element within the RFID or NFC system to possess dual mode Reader / Tag functionality or dual activity rather than one passive and one active component in any system, analogous to the transceiver functionality that exists within radio transmission equipment today.

Several technical problems need to be addressed to realise a dual mode Reader / Tag functionality or NFC systems in which both reader and tag functionality exist to the same level. Firstly, for a dual antenna solution, close proximity of the antennas will result in interference between the antennas. This effect is especially acute for proximity or vicinity coupled systems where the coupling mechanism is magnetic. The solution to this problem would involve either positioning the antennas at mutual magnetic nulls, or including an enable/disable function for the system antenna. Both of these solutions are likely to result in increased complexity, cost and size of the dual mode solution. Secondly, for a single antenna solution, the inherently different properties of the antennas used for reader and/or tag functionality could result in range reduction due to insufficient modulation depth depending on the design of the antenna. The following sections outline the IRT proposed solution for a single antenna dual mode Reader / Tag functionality or NFC system. The IRT proposed solution achieves maximum range performance, with minimal increase in circuit complexity, without a significant size or cost penalty compared to a conventional single mode Reader / Tag system or NFC system. Additional advantages of the suggested architecture are reduced silicon area and reduced power consumption.

2 Proposed Solution Operational Overview

Example 1

An example proposed solution is illustrated in Figure 1. In "Reader" or active mode the resonant antenna (or antennae) is driven with a carrier excitation signal as per a conventional Reader configuration. In "Tag" mode or passive mode (which could be a default condition) a phase locked loop (PLL) is used to provide a local phase-coherent oscillator. The PLL is a second order loop comprising a phase detector, loop filter and VCO. By incorporating a track and hold function between the loop filter and VCO, it is possible to hold the local phase-coherent oscillator signal in the absence of input signal to the phase detector (subject to voltage drift in the track and hold function when in the "hold" mode). A feature of the present invention is to integrate the track and hold with the loop filter as exemplified in Figure 2. If the track and hold and loop filter functions are truly separate, then the output of the loop filter can saturate at either extreme of its range when the negative feedback loop is broken by placing the track and

hold into hold mode. This can cause an increase in loop lock-in time due to the inherent loop filter (lowpass like) response when the negative feedback loop is re-established by placing the track and hold in track mode to re-synchronise with an incoming signal. The loop filter of Figure 2 is placed into hold mode by opening the switch between the phase detector and the input to the filter proper. When open, the filter can be approximated as a floating integrator whose capacitive element will hold the last DC voltage applied to it (neglecting fixed error sources such as leakage currents and offset voltages). This function can be better described as a "filter and hold function". To function correctly, it is essential that the filter is commanded into hold mode only when the loop has completely stabilized and the output of the phase detector is no longer changing.

When phase lock is achieved (as indicated by a lock detect function within the PLL phase detector) the micro-controller is alerted and asserts a signal which commands the track and hold to enter hold mode thereby holding the VCO control voltage within the PLL. The PLL loop is now broken and the VCO output is a phase coherent replica of the reader carrier signal. Clearly, the phase-coherence will slowly degrade over time due to the natural droop of the track-and-hold function. However, the technique does not require perfect phase coherence to operate and in any case the time for which the PLL will be 'free running' is small compared to the droop rate of the envisaged track-and-hold. (Degrading phase coherence will cause a corresponding and steady reduction in modulation depth as seen by the reader.)

The phase-coherent local reference is modulated by the emulated tag data pattern and modulates (either constructively or destructively) the current in the emulated tag antenna. This is reflected back to the external reader through mutual inductive coupling and thereby appears as modulated data at the reader. A key variable in this architecture is the drive level applied to the emulated tag antenna. This level should be dynamically adjustable according to the signal level received from the external reader to avoid the possibility of overloading the external reader receiver input amplifier. We accommodate this by utilising an amplitude levelling loop referenced from the received carrier amplitude detector block. This loop serves to keep the phase inverted drive level at some optimum point which depends on system characteristics.

An additional feature of this approach is the utilisation of the PLL sub-system as part of a synchronous demodulator. When in Reader mode the received modulated carrier from a remote reader (which will not, by definition, be phase-coherent with the local carrier oscillator) can be used to drive the PLL and thereby obtain a phase-coherent local oscillator which is used in conjunction with a synchronous detection of the incoming modulated carrier.

Example 2

Using the dual mode Reader / Tag architecture or NFC system in Tag or passive mode the power detector within the receiving circuitry captures a sampled measurement of the received signal strength. This information can be used, within the controller and AGC, in conjunction with other calibration or predictive data if required, to set and control the output modulation depth, with the modulator and driver, to a desired value using an AGC algorithm. This desired value can take several forms, examples of which are listed, but not limited to, the following cases.

- To provide a constant, e.g., 10% or 100% modulation depth, as perceived by a separate external Reader or NFC system, independent of received signal strength,

i.e. distance between the separate Reader or NFC system and the dual mode Reader / Tag or NFC system.

- To provide a power limiting capability enabling active overload protection for separate external Readers or NFC systems, for example, when the external Reader or NFC System and the Dual mode Reader / Tag or first NFC system are in extremely close proximity.

3 Benefits of Proposed Solution

The proposed solution has a major benefit over conventional passive Tag operation and for the evolution of NFC systems. With a conventional passive Tag the modulation depth is limited by the energy of the incoming signal. With the proposed solution this limitation is removed, as the modulation depth is dependent on the energy that can be generated by the driver stage, which is independent of any external signals or circuitry.

The example proposed solution may also be used with other forms of antenna or multiple antennas, and other coupling mechanisms, such as far field electromagnetic, acoustic, optical etc.

Other examples of the proposed solution would include but are not limited to,

- Injection Locking receiving circuitry
- Parametric amplifying receiving circuitry
- Delay lock loop receiving circuitry

4 Claims

1. A Reader or NFC architecture that can emulate TAG functionality.
2. A dual mode Reader / Tag architecture or NFC architecture using a phase locking technique for the Tag or passive mode of operation.
3. A dual mode Reader / Tag architecture or NFC system where the functionality modulation depth is independent of the energy of the incoming or separate Reader or NFC signal.
4. A dual mode Reader / Tag architecture or NFC architecture where the functionality modulation depth that is read by an external reader or NFC system can be set to a predefined value.
5. A dual mode Reader / Tag architecture where the functionality modulation depth hat is read by an external reader or NFC system can be set to provide overload protection for the external Reader or NFC system.
6. A reader or NFC system capable of providing synchronous demodulation of a received signal consisting a local phase locked loop said phase locked loop phase-synchronising with the incoming signal.

Figure 1: IRT Dual Mode Reader / Tag Solution or NFC System

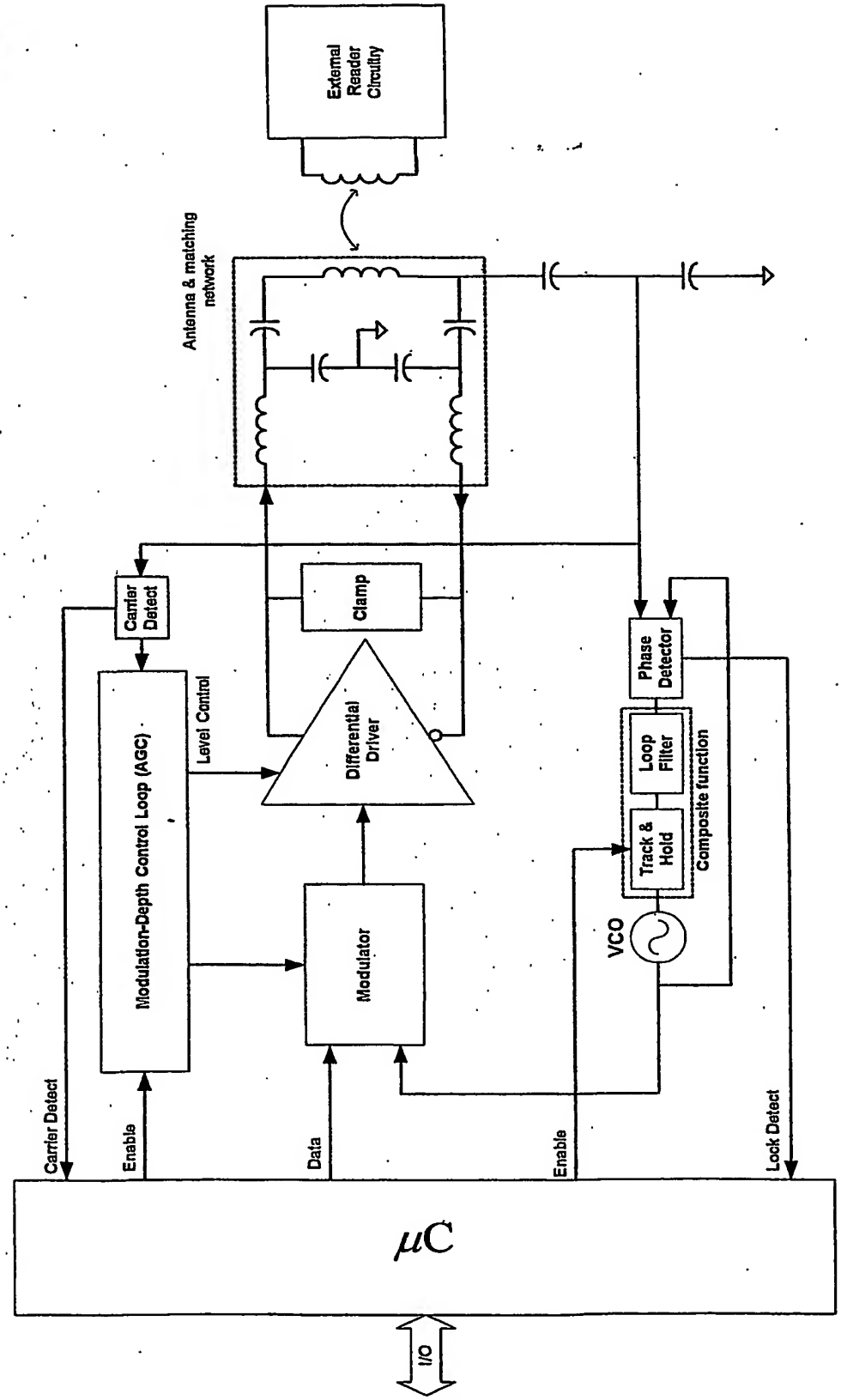

Figure 2: Composite Track & Hold and Loop Filter